REMARKS

Claims 56 - 83 are presently pending. The Examiner has objected to Claim 81 because of the phrase, see line 1. Claims 56 – 58, 60 – 81 and 82 are rejected under 35 U.S.C. §102(b) as being anticipated by Cake *et al.* ('121) hereinafter Cake. Claim 59 is rejected under 35 U.S.C. §103(a) as being unpatentable over Cake in view of Cheng ('428). Claim 83 is rejected under 35 U.S.C. §103(a) as being unpatentable over Cake in view of Watson ('322).

By this Amendment, Applicant has addressed the objection to Claim 81 and entered minor amendments to Claim 56. For the reasons set forth more fully below, the subject application is deemed to properly present claims patentable over the prior art. Reconsideration, allowance and passage to issue are respectfully requested.

The present invention addresses the need in the art for an improved sigma-delta or delta-sigma modulator.

The invention is set forth in Claims of varying scope of which Claim 56 is illustrative. Claim 56 recites:

> 56. A delta-sigma modulator comprising:
> a loop filter;
> a comparator coupled to the loop filter; and
> a switch **coupled to said comparator and said filter**, said switch comprising:
> first means for providing a first set of first and second complementary intermediate signals;
> second means for providing a second set of third and fourth complementary intermediate signals;
> third means responsive to the first set of signals for providing complementary output signals;
> fourth means responsive to the second set of signals for providing complementary output signals; and
> fifth means for selectively activating the third means or the fourth means in response to a control signal **to switch signals from said filter in response to signals from said comparator**. (Emphasis added.)

None of the references, taken alone or in combination, teach, disclose or suggest the invention as presently claimed. That is, none of the references teach, disclose or suggest a

delta-sigma modulator having the unique arrangement with a loop filter, comparator and switch as presently claimed.

In the rejections of the Claims, the Examiner relied primarily on Cake. The Examiner suggests that in Fig. 11, Cake shows a resonator which the Examiner equates with a 'loop filter', a comparator and a switch as claimed.

However, Cake clearly does not show an arrangement in which the switch is coupled to the filter so that the switch is effective to switch signals from the filter in response to signals from the comparator as presently claimed. In this connection, it should be noted that the transistors 613 – 616 of Cake provide a cascade differential amplifier, not a filter. (See col. 6, lines 27 – 33.)

Inasmuch as the objection to Claim 81 has been cured, the present Claims are submitted as being in proper form for allowance. Accordingly, reconsideration, allowance and passage to issue are respectfully requested.

Respectfully submitted,
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